(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: 0 373 360 B1

(12) # EUROPEAN PATENT SPECIFICATION

(45) Date of publication of patent specification: 04.10.95 Bulletin 95/40

(51) Int. Cl.[6]: H01L 21/768, H01L 23/522

(21) Application number: 89120666.6

(22) Date of filing: 08.11.89

(54) **Method and structure for providing improved insulation in VLSI and ULSI circuits.**

(30) Priority: 16.12.88 US 286443

(43) Date of publication of application: 20.06.90 Bulletin 90/25

(45) Publication of the grant of the patent: 04.10.95 Bulletin 95/40

(84) Designated Contracting States: DE FR GB

(56) References cited:
EP-A- 0 043 014
IBM TECHNICAL DISCLOSURE BULLETIN, vol. 32, no. 5B, October 1989, New York, US; pages 418-419; "METHOD TO IMPROVE DIELECTRIC PROPERTIES OF INSULATORS"
IBM JOURNAL OF RESEARCH AND DEVELOPMENT, vol. 29, no. 3, May 1985, New York, US; pages 277-288; P. COTTRELL & E. BUTURLA: "VLSI WIRING CAPACITANCE"

(73) Proprietor: International Business Machines Corporation
Old Orchard Road
Armonk, N.Y. 10504 (US)

(72) Inventor: Roberts, Stanley
23 Kingsland Terrace
Burlington Vermont 05401 (US)
Inventor: Kaanta, Carter Welling
Grandview Road
Colchester Vermont 05446 (US)

(74) Representative: Schäfer, Wolfgang, Dipl.-Ing.
IBM Deutschland
Informationssysteme GmbH
Patentwesen und Urheberrecht
D-70548 Stuttgart (DE)

EP 0 373 360 B1

Description

This invention relates generally to a method and structure for reducing the capacitive coupling either between lines on the same layer (intralayer) or between lines on superposed layers (interlayer) in VLSI or ULSI circuits. In more particular aspects the present invention relates to a method and structure for yielding an effectively reduced dielectric constant between lines on the surface of a given VLSI or ULSI chip or on lines mounted on various layers or surfaces on VLSI or ULSI structures utilizing air, other gasses, or a partial vacuum as a dielectric medium.

It has been conventional prior art practice in integrated circuit chip production to utilize materials such as silicon dioxide, silicon nitride, polyimides and certain other organic materials as dielectric materials interposed between the metal lines on a given layer and between various layers of metalization in the wiring portion of the integrated circuit chip.

EP-A-043 014 includes methods and apparatus for providing relatively long conductors on integrated chips with substantially reduced RC time constants. The preferred mode utilizes a substrate having a metallization pattern wherein etching or milling into the substrate creates a cavity with a metallization conductor disposed in the mouth of the cavity, said cavity being metallized to provide the second conductor. A similar structure may be formed by utilizing orientation dependent etchant which attacks the surface much quicker than the surface to provide an etched V-shaped cavity wherein the first conductor is still an elongated metallization segment in the mouth of the V, and the V is metallized to provide the second conductor. Also, a single conductor, such as the elongated metallization strip may be extended to a conductor on the reverse side of the substrate by providing a pyramid shaped hole from the first conductor through the substrate, which hole is metallized to extend the first conductor to the second conductor via the hole in the substrate.

However, as the integrated circuit technology progresses into a Very Large Scale Integration (VLSI) and beyond to Ultra Large Scale Integration (ULSI) the spacing between the metal lines on any given plane and the interplanar spacing of metal lines becomes less and less, extending into the submicron range for intralayer spacing. This increases the capacitive losses between the lines and gives rise to a need for the space between the lines having improved dielectric properties; i.e., with a dielectric constant as low as possible.

The dielectric constants of silicon nitride (which is about 7.0), CVD silicon dioxide (which is 3.9), and polyimides (which are about 3.6), are not sufficiently low to provide acceptable insulation in these submicron ranges; hence, it is necessary to provide a medium with improved dielectric properties, e.g. a constant of 2.0 or less in the intraplanar spaces between lines and interplanar spaces between lines at different levels.

IBM Technical Disclosure Bulletin, Vol. 32, No. 5B, October 1989, pp. 418-419, "Method to Improve Dielectric Properties of Insulators" describes how the effective dielectric constant of existing insulators can be lowered through process modification as opposed to the use of a new generation insulator with a lower intrinsic dielectric constant. Rather than using a blanket insulator, the insulator is patterned to support the interconnection metal at intervals along its length and at the interlevel via locations. Doing so allows air to become a significant portion of the effective dielectric constant. Since air has a much lower dielectric constant than existing organic or inorganic insulators, the effective dielectric constant is lowered.

The invention as claimed is intended to remedy these drawbacks and solves the problem of providing an improved insulation.

Accordingly, a method and structure for providing an insulating electrical space between two lines on a layer of material or between lines on adjacent superposed layers of material are provided as defined by claims 1 and 9, respectively. According to this invention a base member is formed having a plurality of support members extending upwardly from said base member. A removable material is deposited on said base member and around said support members. A cap member of insulating material is then disposed over said support members and said removable material. Access openings are formed in at least one of the base member or the cap member communicating with said removable material. The removable material is removed through the access openings to thereby define a space between said cap member and said base member and between said support members. During this step a partial vacuum (in which some inert gas may be dispersed) may be created in the space vacated by the removable material.

The access openings are then filled in so as to provide a sealed space between the cap member and the base member which has a very low dielectric constant.

For a better understanding of the present invention and its further objects and advantages, preferred embodiments of the invention are described below with reference to the accompanying drawings, in which:

Figures 1a through 1h — are perspective sectional views somewhat diagrammatic showing various steps in one method of producing a structure according to this invention; and

Figures 2a through 2m — are perspective sectional views somewhat diagrammatic showing various steps in another method of producing a structure according to this invention.

Referring now to the drawing and for the present Figures 1a through 1f the various steps in producing a structure according to one method of the present invention are depicted, somewhat diagrammatically. As shown in Figure 1a an insulating substrate material 10 such as SiO_2 is provided which may overlie the devices on a VLSI or ULSI integrated circuit chip (not shown). The insulating material 10 has disposed thereon metal lines 12 which may be aluminum or other metal which have been patterned by conventional photolithographic techniques to provide the desired wiring structure on top of the insulating layer 10. A layer of removable material 14 is deposited atop the substrate material 10 and around the metal lines 12. The preferred material for this is a poly-para-xylylene, (PPX) an organic polymer sold by Union Carbide Corporation, under the Trademark Parylene N, which can be readily selectively removed under certain specific conditions as will be described presently. However, other removable materials which have the property of being etched or consumed at a rate significantly and substantially faster than any of the material surrounding it (i.e. the metal and silicon dioxide) can also be used. Other such additional materials include spun on glasses which can be removed in HF acid etch.

When parylene is used, this can be deposited by chemical vapor deposition (CVD) techniques which are well known in the art. For example, CVD deposition by the Gorham method is a very good technique. This is done after first optionally applying an adhesion promoter such as AllOO sold by Shipley Co. Thereafter the PPX is applied by heating the PPX source material to 165°C and passing the vapor through a furnace in a tube at 425°C and thereafter depositing the heated vapor onto the substrate in a chamber at 5.32 Pa (40 millitorr) pressure and room temperature. When the material has been deposited it is planarized by a suitable technique such as an etch back or other planarization techniques so that the top surface is flush with the top of the metal lines 12. One such etch back technique is as follows: A layer of planarizing resist material, such as AZ1350 sold by Shipley Co. is spun applied and then baked at about 120°C. This is followed by etching in O_2 in a reactive ion etching tool. This etching continues until all the resist has been removed and the resulting structure is a planarized surface of parylene 14 and metal lines 12. This structure is shown in Figure 1b.

An insulating cap material 16 is then deposited on top of the planarized parylene surface and metal, which cap preferably also is silicon dioxide which can be deposited by conventional techniques. In one such technique the SiO_2 is deposited in an AME 3300 deposition tool using 1.9% SiH_4 with He at 3000 sccm, and N_2O at 2500 sccm, carried out at a pressure of 266 Pa (2.0 Torr), a temperature of 340°C, and a power of 150 watts. Following this, a layer of photoresist material 18 is deposited on top of the insulating material 16 and patterned by conventional photolithographic processes so as to provide the desired opening configurations 19 for access to the metal lines and to parylene material as will become clear presently and as shown in Figure 1c.

The revealed SiO_2 material on the cap 16 underlying the openings 19 is removed by any conventional etching technique utilizing the unexposed remaining photoresist material 18 as a mask. One such technique being as follows: The SiO_2 is etched in an AME 8100 etching tool using CHF_3 at 75 sccm, and CO_2 at 8 sccm, carried out at 5.32 Pa (40 millitorr), at ambient temperature and at a power of 1200 watts. The remaining photoresist 18 is then removed. This will result in the structure shown in Figure 1d. As can be seen in Figure 1d there are a plurality of openings one of which is shown at 20, which extends through the cap material 16 to the underlying metalization layer 12, while other openings, one of which is shown at 22, extend through the insulating cap material 16 and communicate with the underlying parylene material 14. The openings 20 will be used to provide interlayer contact and the openings 22 will be used as access openings to remove the material 14 as will be described presently.

A metal such as tungsten 24 is deposited in the openings 20 as shown in Figure 1e which can be effectively accomplished by selective deposition as follows: The tungsten is deposited in a Varian 5100 tool, using WF_6 at 10 sccm, H_2 at 200 sccm, SiH_4 at 10 sccm and at a temperature of about 300°C.

Following the tungsten deposition, the parylene material is removed through the access openings by heating the entire structure in an O_2 rich atmosphere at a temperature of about 200°C. This will cause the perylene material 14 to react with the oxygen in the atmosphere and essentially turn to gas and be expelled through the access openings 22 leaving spaces 25 between the metal lines 12 and between the base layer 10 and the cap 16 as shown in Figure 1f.

At this point in the process, the access openings 22 are filled, preferably by a technique of CVD deposition of SiO_2 utilizing an inert carrier gas at a pressure of about 13.3 Pa (100 millitorr). This is quite a low pressure and any ambient atmosphere which is contained within the spaces between the base 10 and cap 16 and between metal lines 12 is replaced by the vacuum and a certain small amount of whatever carrier gas is used to perform chemical vapor deposition of the SiO_2. This chemical deposition of SiO_2 will effectively close the access openings 22, and, since the process is being carried out at the very low pressure of 13.3 Pa (100 millitorr) with inert carrier gas the resulting space between the metal lines 14 has a very low pressure therein containing only small amounts of inert gas. This will give a dielectric constant of 2.0 or less.

In the deposition of the SiO_2 on the cap 16 to close the access openings 22 there will also be a layer 26

of the SiO_2 material deposited on the top thereof as shown in Figure 1g. This layer 26 is then blanket etched by the reactive ion etching (R.I.E.) process as described above to expose the top of the tungsten as shown in Figure 1h, which can then act as a via or stud for interlayer connection. The desired metallization can then be applied to the top of the cap layer 16, and the whole process repeated if additional layers of metallizations are desired.

Referring now to Figures 2a through 2m the steps in another embodiment of this invention are shown which is particularly effective for providing not only intralayer insulation between two metal lines on a given layer, but also is especially effective for providing interlayer insulation of metal lines on two superposed layers of insulation.

In this embodiment, a first layer of metal 31 such as tungsten is blanket deposited onto an insulating substrate 30 such as silicon dioxide by any suitable deposition technique. One such technique is a sputter process utilizing a Perkins-Elmer 4450 tool at 600 watts D.C. magnetron sputtering at 1.33-3.99 Pa (10-30 millitorr) pressure with a bias of between 0 and 60 volts. Thereafter a layer of aluminum is blanket deposited onto the tungsten by any suitable process. This aluminum can be deposited by using an RF evaporation source at a pressure of about 133 µPa (1 microtorr). On top of the aluminum metal 32, a silicon dioxide layer 34 is deposited as previously described. On top of the silicon dioxide layer 34 a layer of silicon nitride 36 is deposited. The silicon nitride deposition is preferably done in an ASM tool utilizing SiH_4 at 175 sccm, and NH3 at 325 sccm, carried out at a pressure of 266 Pa (2 torr), a temperature of 375°C, and a power of 160 watts. This is the starting structure and is shown in Figure 2a.

The overlying silicon nitride layer 36 is then patterned by convention photolithographic techniques and reactive ion etched to provide the structure shown in Figure 2b wherein there are a series of pads of silicon nitride 36 atop the silicon dioxide layer 34.

A layer of photoresist material 38 is then deposited over the surface of the structure shown in Figure 2b and patterned and developed in a conventional manner to provide the pattern shown in Figure 2c. The pattern of the photoresist 38 corresponds to the desired pattern of lines which will be etched in the underlying metal layer 32 as will become apparent presently.

The silicon nitride pads 36 have been intentionally made slightly wider than the width of the photoresist pattern material 38 so as to provide a self-aligning feature which is well known in the art. At this point the excess nitride 36 is trimmed in an AME Hexode tool using CHF_3 at 75 sccm, and O_2 at 10 sccm, carried out at a power of 800 watts. This provides the structure shown in Figure 2d.

At this point the structure is etched using the undeveloped photoresist pattern 38 as a mask, the etching first being through the exposed silicon dioxide 34 down to the exposed metal layer 32 and thereafter the aluminum metal layer 32 is etched so as to reveal the underlying tungsten 31 and provide a line pattern as shown in Figure 2e. This etching takes place by the following process: First the SiO_2 is etched as previously described until it is completely removed to expose the aluminum metal. The aluminum is etched in an AME 8300 tool using a multistep process as follows:
first in CF_4 at 40 sccm, carried out at a pressure of 3.33 Pa (25 millitorr) with a D.C. bias of 25 volts;
thereafter in $BC1_3$ at 140 sccm, $C1_2$, at 30 sccm, CH_3 at 15 sccm, and CH_4 at 15 sccm, carried out at a pressure of 4 Pa (30 millitorr) and a D.C. bias of - 160 volts until the unmasked aluminum is removed.

At this point the remaining photoresist 38 is stripped away. The silicon dioxide which underlies the photoresist but which is not covered by the Si_3N_4 pads 36 is removed by etching as previously described, the pads 36 acting as etch marks on the SiO_2 layer 34 and the tungsten 31 acting as an etch mask on the SiO_2 layer 30. The tungsten 31 is then removed by any suitable means, such as by reactive ion etching in a suitable gas such as SF_6 at a rate of 150 nm per minute. This will provide the structure as sown in Figure 2f. At this stage in the process underlying aluminum metal lines 32 have disposed thereon stanchions 40, two of which is shown in Figure 2f, each stanchions being comprised of a silicon nitride layer 36 and a silicon dioxide layer 34.

Removable material 41 such as parylene is deposited (as previously described) onto the surface of the substrate 30 so that it fills between the metal lines 32 and around the stanchions 40, and is planarized back as previously described to the structure shown in Figure 2g. (The silicon nitride need not remain after this point in the process, and if desired can be removed as a part of the planarization operation using conventional techniques as previously described.)

A cap layer 42 of silicon dioxide is then blanket deposited on top of the structure shown in Figure 2h. A layer of photo resist is deposited on the cap layer 42 and patterned and developed as described in the previous embodiment to provide for the necessary via and access openings. Via openings, one of which is shown at 44, and access openings 46, are etched through the silicon dioxide cap layer 42 by the technique as previously described, the via openings being located above the stanchions 40 and the removal or access openings 46 being located above the removable material 41 and the photoresist material removed to provide the structure as shown in Figure 2i. It should be noted that the etching of the via hole 44 proceeds through both the oxide

cap material 42 and the silicon nitride 36 and the underlying oxide material 34 to the metal 32. This etching process is carried out in an AME 8100 etching tool wherein the SiO_2 is first etched as previously described to remove the SiO_2 revealing the silicon nitride. The silicon nitride is then etched in an AME Hexode tool as previously described to reveal the SiO_2. This final layer of SiO_2 is etched as previously described to reveal the underlying aluminum lines.

As in the previously described embodiment, metal 48 is deposited into the via 44 to provide an interconnection which preferably is tungsten as previously described and shown in Figure 2j. The material 41 is then removed as previously described. If the material is parylene it is removed by heating the structure in an O_2 atmosphere at about 200°C or less until the material is removed as shown in Figure 2k providing spaces 50 between the lines 32 and between the base 30 and cap 42. If the material is spun on glass it can be etched out by a solution of 100 parts HNO_3, 100 parts H_2O, and 1 part HF. If other material is used it can be suitably removed by selecting enchants that do not significantly react either with the silicon dioxide, or the silicon nitride or the metal.

The structure is then subjected to a CVD silicon dioxide deposition as previously described to close the access openings 46 and provide a layer 52 on top of cap 42 which when done at a pressure of 13.3 Pa (millitorr) will result in a relatively low pressure spaces 50 as shown in Figure 2l. The layer 52 is then etched back as previously described to provide the resulting structure shown in Figure 2m.

This particular embodiment is particularly adapted not only for use with intralayer insulation but also interlayer insulation in that there is provided a plurality of stanchions or supports 40 separating the base layer 30 and cap layer 42, which stanchions are comprised of a layer of silicon dioxide and silicon nitride overlying the metal lines 32 thus increasing the space 50 constituting the space between the layer 32 and the cap 42.

Claims

1. A method of providing an electrically insulating medium between a base insulating member and a superposed insulating cap member comprising the steps of;
providing said base member (10; 30), preferably silicon dioxide;
forming a plurality of support means (12; 31/32, 40) extending upwardly from said base member, said support means comprising at least a metal layer;
depositing a selectively-removable material (14; 41), preferably poly-para-xylylene or spun on glass on said base member and on said support means, planarizing said removable material so that at least the upper surface of portions of said support means and the upper surface of said removable material are coplanar;
providing said cap member (16; 42) on the thus obtained planarized surface;
forming access opening means (22; 46) in said cap member communicating with said removable material;
removing said removable material through said access opening means without appreciably removing any of the base member or the cap member or the support means to thereby define a space between said base member and said cap member and around said support means;
thereby providing a space between said members and around said support means of a low dielectric constant.

2. The method as defined in claim 1 wherein said support means includes a plurality of metal lines (12; 31/32) formed on an insulating substrate.

3. The method as defined in claim 2 wherein said cap member is an insulating material, preferably silicon dioxide.

4. The method as defined claim 3 wherein said cap member is deposited directly onto said metal lines and said removable material.

5. The method as defined in claim 3 wherein said support means include a plurality of stanchions (40), preferably formed by deposition and selective etching of insulating materials, on said metal lines; and wherein said cap member is deposited onto said stanchions and said removable material.

6. The method as defined in any one of the preceding claims 3 to 5 further providing via openings (20; 44) through said insulating cap member, and filling said openings with a metal, thus contacting said metal lines.

7. The method as defined in any one of the preceding claims 3 to 6 wherein said access openings are sealed by depositing an insulating material in said access openings.

8. The method as defined in claim 7 wherein a vacuum is created in said space during the step of depositing the insulating material in said access openings.

9. A VLSI or ULSI structure comprising, a dielectric base member (10, 30),
a plurality of spaced metal conducting lines (12; 31, 32) formed on said base members and extending upwardly therefrom;
a dielectric cap member (16, 42) superposed on said base member and supported at least in part by said metal lines,
said cap member, said base member and said metal lines defining a plurality of spaces therebetween, each of said spaces having a dielectric constant of less than 2.0.

10. The structure as defined in claim 9 wherein said cap member is supported directly on said metal lines.

11. The structure as defined in claim 9 or 10 wherein a plurality of insulating stanchions (40) are formed on said metal lines, and said cap member is supported on said insulating stanchions.

12. The structure as defined in any one of the preceding claims 9 to 11 further characterized by metal vias (44) extending through said cap member and contacting said metal lines.

13. The structure as defined in any one of the preceding claims 9 to 12 further characterized by access openings (22, 46) in said cap member, said access openings being sealed with an insulating material.

Patentansprüche

1. Verfahren zur Herstellung eines elektrisch isolierenden Mediums zwischen einem isolierenden Basiselement und einem darübergeschichteten isolierenden Abdeckelement, das folgende Schritte beinhaltet:
Bereitstellen des Basiselementes (10; 30), vorzugsweise Siliciumdioxid;
Bilden einer Mehrzahl von Trägermitteln (12; 31/32, 40), die sich von dem Basiselement aus nach oben erstrecken, wobei die Trägermittel wenigstens eine Metallschicht beinhalten;
Aufbringen eines selektiv entfernbaren Materials (14; 41), vorzugsweise Polyparaxylylen oder aufgeschleudertes Glas, auf dem Basiselement und auf den Trägermitteln, Planarisieren des entfernbaren Materials, so daß wenigstens die Oberseite von Bereichen der Trägermittel und die Oberseite des entfernbaren Materials koplanar sind;
Erzeugen des Abdeckelements (16; 42) auf der so erhaltenen planarisierten Oberfläche;
Bilden von Zugriffsöffnungsmitteln (22; 46) in dem Abdeckelement, die mit dem entfernbaren Material in Verbindung stehen;
Entfernen des entfernbaren Materials durch die Zugriffsöffnungsmittel hindurch, ohne etwas von dem Basiselement oder dem Abdeckelement oder den Trägermitteln merklich zu entfernen, um dadurch einen Zwischenraum zwischen dem Basiselement und dem Abdeckelement und um die Trägermittel herum zu definieren;
wodurch ein Zwischenraum zwischen den Elementen und um die Trägermittel herum mit einer niedrigen Dielektrizitätskonstante bereitgestellt wird.

2. Verfahren wie in Anspruch 1 definiert, wobei die Trägermittel eine Mehrzahl von Metallbahnen (12; 31/32) beinhalten, die auf einem isolierenden Substrat ausgebildet sind.

3. Verfahren wie in Anspruch 2 definiert, wobei das Abdeckelement aus einem isolierenden Material besteht, vorzugsweise Siliciumdioxid.

4. Verfahren wie in Anspruch 3 definiert, wobei das Abdeckelement direkt auf die Metallbahnen und das entfernbare Material aufgebracht wird.

5. Verfahren wie in Anspruch 3 definiert, wobei die Trägermittel eine Mehrzahl von Stützen (40), die vorzugsweise durch Deposition und selektives Ätzen von isolierenden Materialien erzeugt werden, auf den

Metallbahnen beinhalten; und
wobei das Abdeckelement auf die Stützen und das entfernbare Material aufgebracht wird.

6. Verfahren wie in irgendeinem der vorhergehenden Ansprüche 3 bis 5 definiert, bei dem des weiteren Durchkontaktöffnungen (20; 44) durch das isolierende Abdeckelement hindurch erzeugt und die Öffnungen mit einem Metall gefüllt werden, womit die Metallbahnen kontaktiert werden.

7. Verfahren wie in irgendeinem der vorhergehenden Ansprüche 3 bis 6 definiert, wobei die Zugriffsöffnungen durch Aufbringen eines isolierenden Materials in die Zugriffsöffnungen versiegelt werden.

8. Verfahren wie in Anspruch 7 definiert, wobei in dem Zwischenraum während des Schritts des Aufbringens des isolierenden Materials in den Zugriffsöffnungen ein Vakuum erzeugt wird.

9. VLSI- oder ULSI-Struktur, mit einem dielektrischen Basiselement (10, 30),
einer Mehrzahl von mit Abstand voneinander angeordneten leitenden Metallbahnen (12; 31, 32), die auf den Basiselementen gebildet sind und sich von diesen aus nach oben erstrecken;
einem dielektrischen Abdeckelement (16, 42), das auf das Basiselement geschichtet ist und wenigstens teilweise von den Metallbahnen getragen ist,
wobei das Abdeckelement, das Basiselement und die Metallbahnen eine Mehrzahl von Zwischenräumen zwischen denselben definieren,
wobei jeder der Zwischenräume eine Dielektrizitätskonstante von kleiner als 2,0 aufweist.

10. Struktur wie in Anspruch 9 definiert, wobei das Abdeckelement direkt auf den Metallbahnen getragen ist.

11. Struktur wie in Anspruch 9 oder 10 definiert, wobei eine Mehrzahl von isolierenden Stützen (40) auf den Metallbahnen ausgebildet ist und das Abdeckelement auf den isolierenden Stützen getragen ist.

12. Struktur wie in irgendeinem der vorhergehenden Ansprüche 9 bis 11 definiert, weiter gekennzeichnet durch Metalldurchkontakte (44), die sich durch das Abdeckelement hindurch erstrecken und die Metallbahnen kontaktieren.

13. Struktur wie in irgendeinem der vorhergehenden Ansprüche 9 bis 12 definiert, weiter gekennzeichnet durch Zugriffsöffnungen (22, 46) in dem Abdeckelement, wobei die Zugriffsöffnungen mit einem isolierenden Material versiegelt sind.

Revendications

1. Procédé d'obtention d'un support isolant électriquement entre un élément isolant de base et un élément de couvercle isolant superposé comprenant les étapes suivantes:
fourniture dudit élément de base (10; 30), de préférence du dioxyde de silicium;
formation d'une pluralité de moyens de support (12; 31/32, 40) s'étendant vers le haut à partir dudit élément de base, ledit moyen de support comprenant au moins une couche métallique;
dépôt d'un matériau pouvant être supprimé de manière sélective (14; 41), de préférence du polyparaxylylène ou étalé sur du verre sur ledit élément de base et sur ledit moyen formant support, de planéification dudit matériau qui peut être supprimé de telle sorte qu'au moins la surface supérieure de parties dudit moyen formant support et la surface supérieure dudit matériau pouvant être supprimé sont coplanaires;
fourniture dudit élément formant couvercle (16; 42) sur la surface plane ainsi obtenue;
formation de moyens (22; 46) formant ouvertures d'accès dans ledit élément formant couvercle communiquant avec ledit matériau pouvant être supprimé;
retrait dudit matériau pouvant être supprimé à travers ledit moyen formant ouverture d'accès sans retirer de manière appréciable l'un de l'élément de base ou de l'élément de couvercle ou le moyen de support afin de définir un espace entre ledit élément de base et ledit élément formant couvercle et autour dudit moyen formant support;
afin de fournir un espace entre lesdits éléments et autour dudit moyen formant support de faible constante diélectrique.

2. Procédé selon la revendication 1 dans lequel ledit moyen formant support comporte une pluralité de lignes métalliques (12; 31/32) formées sur un substrat isolant.

3. Procédé selon la revendication 2 dans lequel ledit élément formant couvercle est en un matériau isolant, de préférence du dioxyde de silicium.

4. Procédé selon la revendication 3 dans lequel ledit élément formant couvercle est déposé directement sur lesdites lignes métalliques et ledit matériau pouvant être retiré.

5. Procédé selon la revendication 3 dans lequel ledit moyen formant support comporte une pluralité de barres (40), de préférence formées par dépôt et attaque sélective de matériaux isolants, sur lesdites lignes métalliques; et

dans lequel ledit élément formant couvercle est déposé sur ladite barre et ledit matériau pouvant être retiré.

6. Procédé selon l'une quelconque des revendications précédentes 3 à 5 comprenant en outre des ouvertures (20; 44) à travers ledit élément formant couvercle isolant, et le remplissage desdites ouvertures avec un métal, par conséquent en contact avec lesdites lignes métalliques.

7. Procédé selon l'une quelconque des revendications précédentes 3 à 6 dans lequel lesdites ouvertures d'accès sont fermées en déposant un matériau isolant dans lesdites ouvertures d'accès.

8. Procédé selon la revendication 7, dans lequel un vide est créé dans ledit espace au cours de l'étape de dépôt de matériau isolant dans lesdites ouvertures d'accès.

9. Structure VLSI ou ULSI comprenant un élément de base diélectrique (10, 30),

une pluralité de lignes conductrices métalliques espacées (12; 31, 32) formées sur lesdits éléments de base et s'étendant vers le haut de ceux-ci;

un élément de couvercle diélectrique (16, 42) superposé audit élément de base et supporté au moins en partie par lesdites lignes métalliques,

ledit élément de couvercle, ledit élément de base et lesdites lignes métalliques définissant une pluralité d'espaces entre eux,

chacun desdits espaces ayant une constante diélectrique inférieure à 2,0.

10. Structure selon la revendication 9, dans laquelle ledit élément formant couvercle est supporté directement sur lesdites lignes métalliques.

11. Structure selon la revendication 9 ou 10 dans laquelle une pluralité de barres isolantes (40) sont formées sur lesdites lignes métalliques, et ledit élément formant couvercle est supporté sur lesdites barres isolantes.

12. Structure selon l'une quelconque des revendications précédentes 9 à 11 caractérisée en outre par des traversées métalliques (44) s'étendant à travers ledit élément formant couvercle et en contact avec lesdites lignes métalliques.

13. Structure selon l'une quelconque des revendications précédentes 9 à 12 caractérisée en outre par des ouvertures d'accès (22, 46) dans ledit élément formant couvercle, lesdites ouvertures d'accès étant fermées avec un matériau isolant.

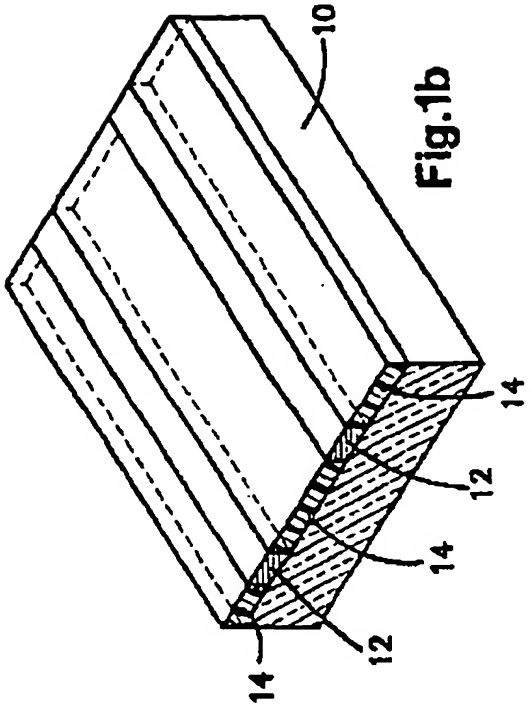

Fig.1b

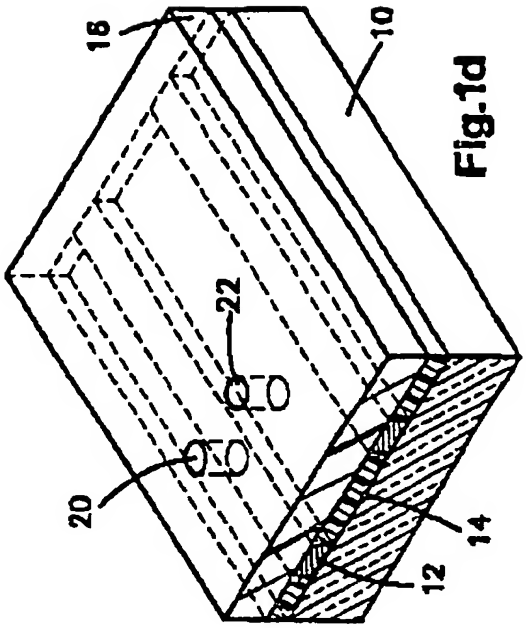

Fig.1d

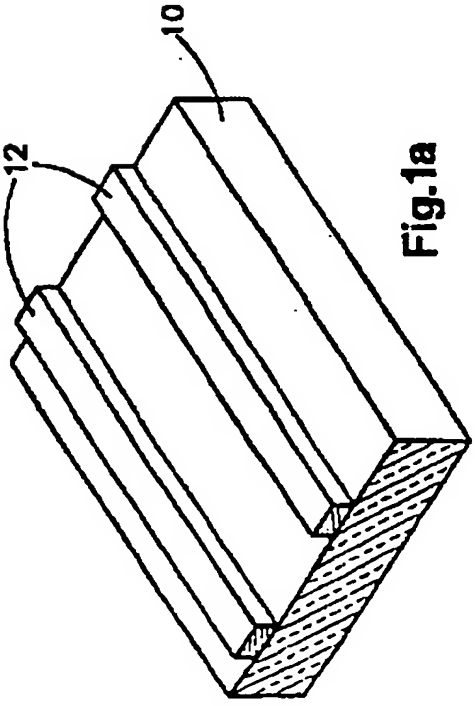

Fig.1a

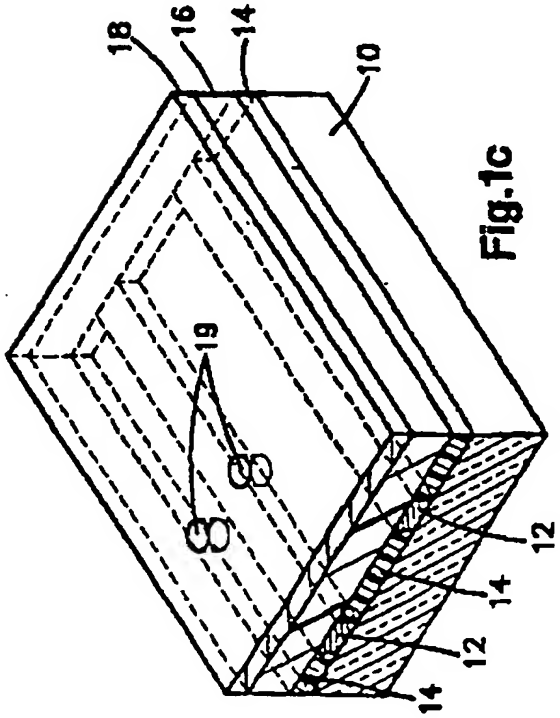

Fig.1c

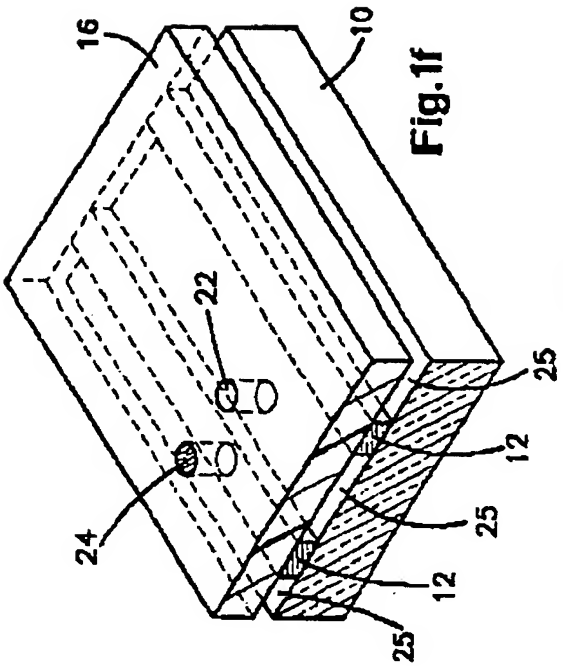

Fig.1f

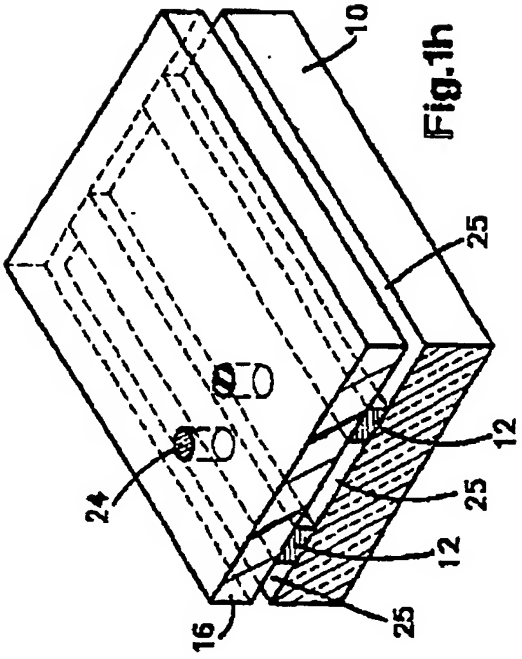

Fig.1h

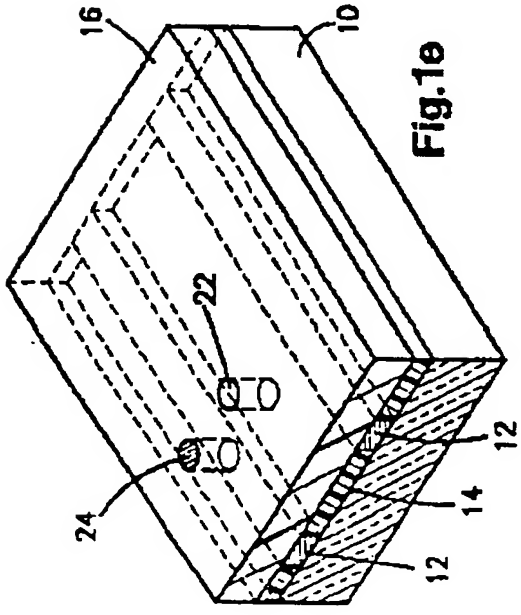

Fig.1e

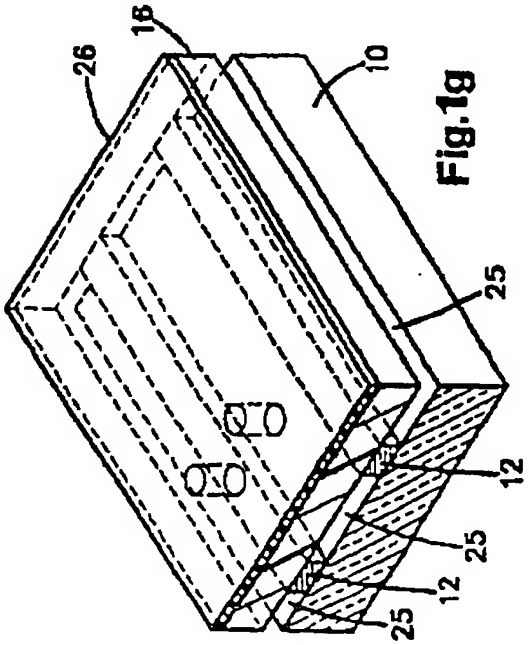

Fig.1g

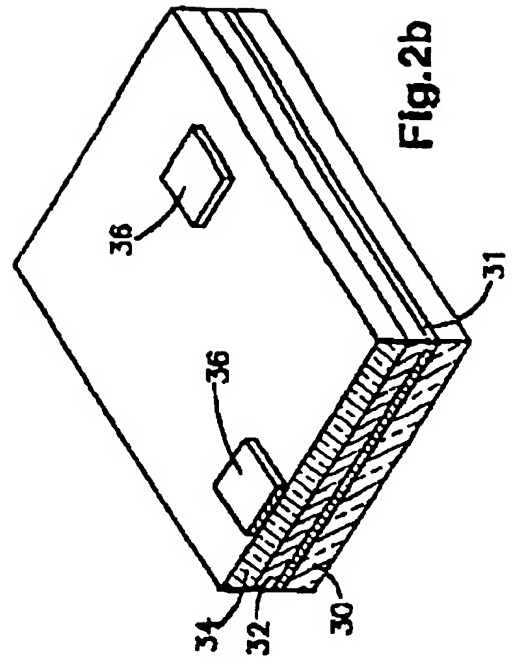

Fig.2b

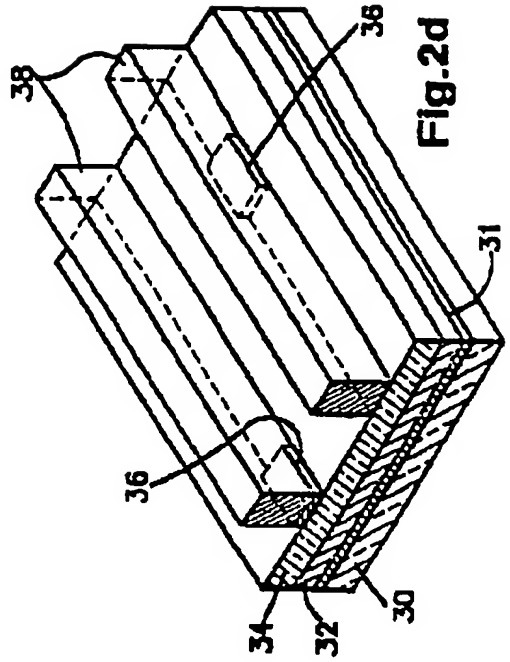

Fig.2d

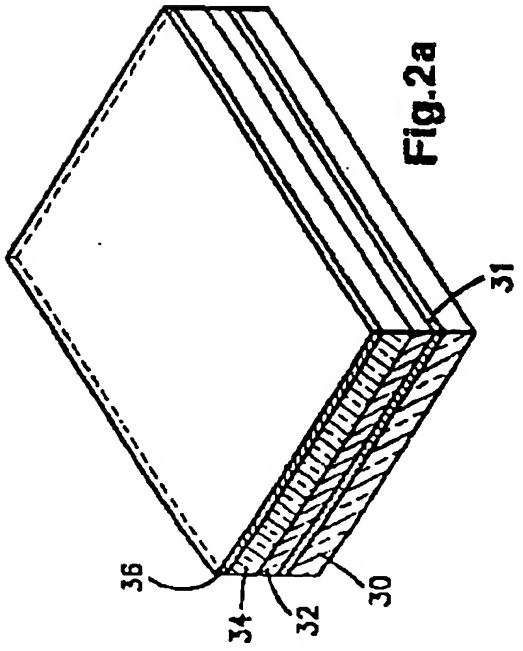

Fig.2a

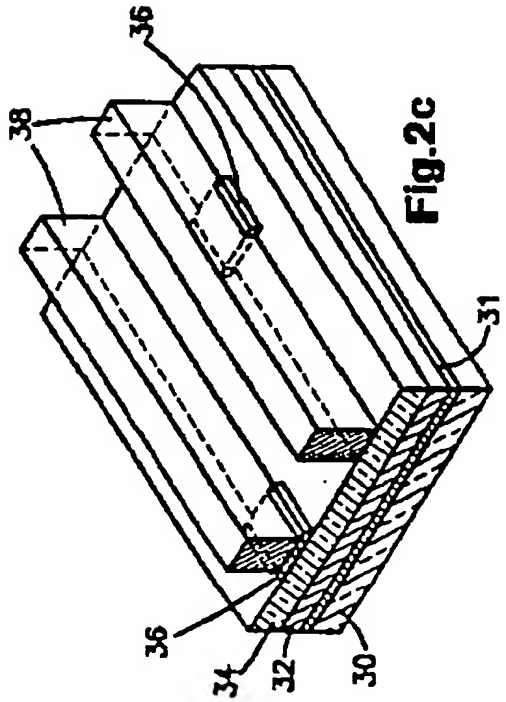

Fig.2c

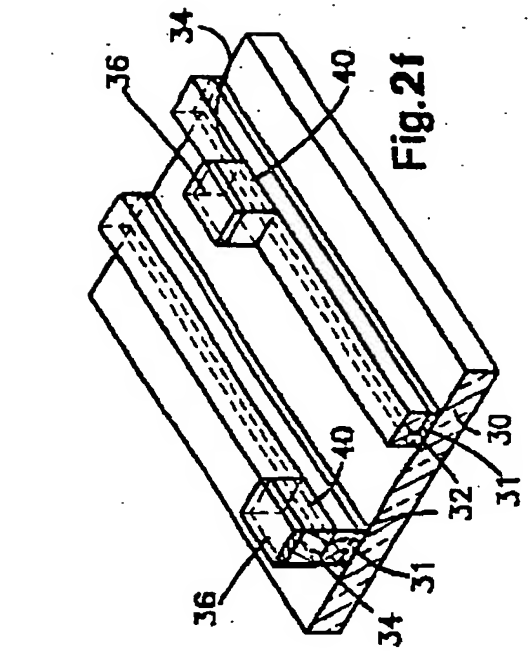

Fig.2f

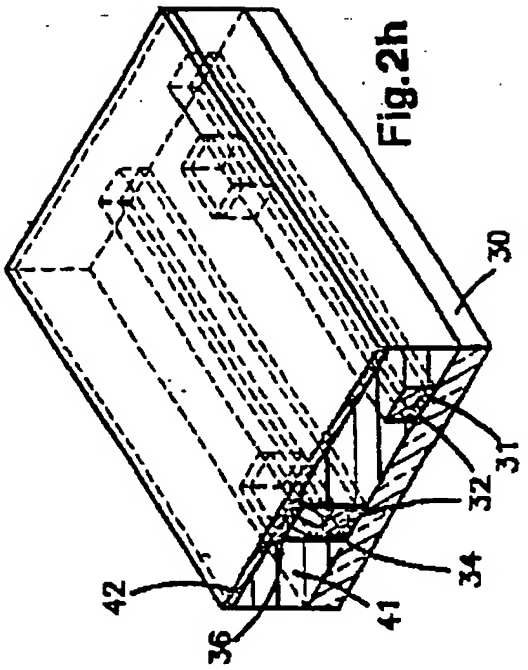

Fig.2h

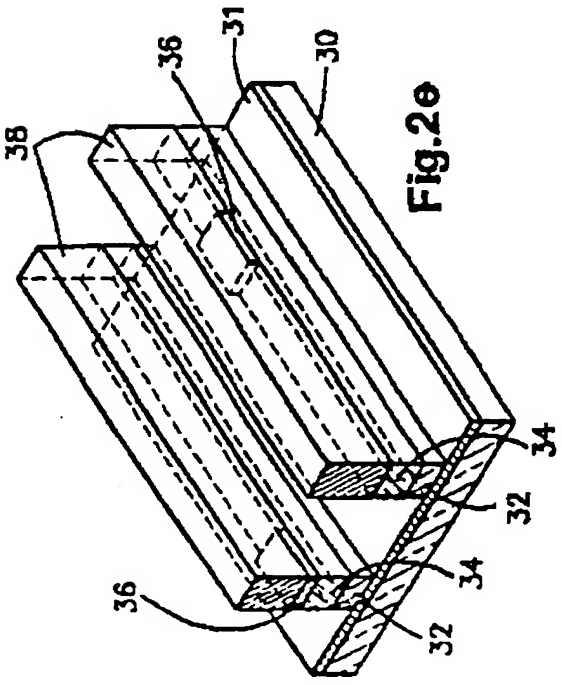

Fig.2e

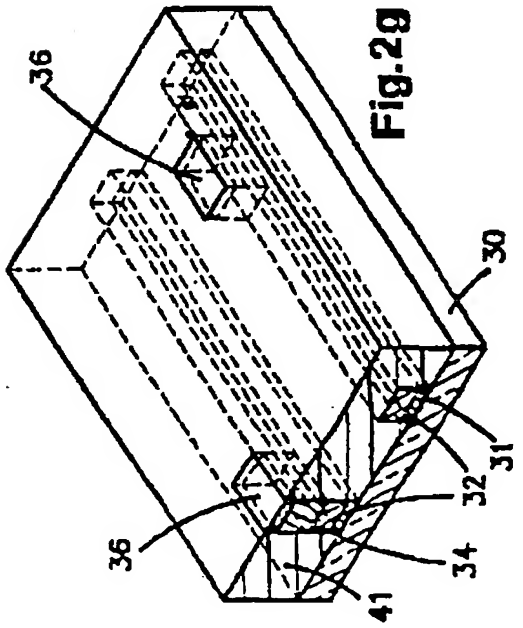

Fig.2g

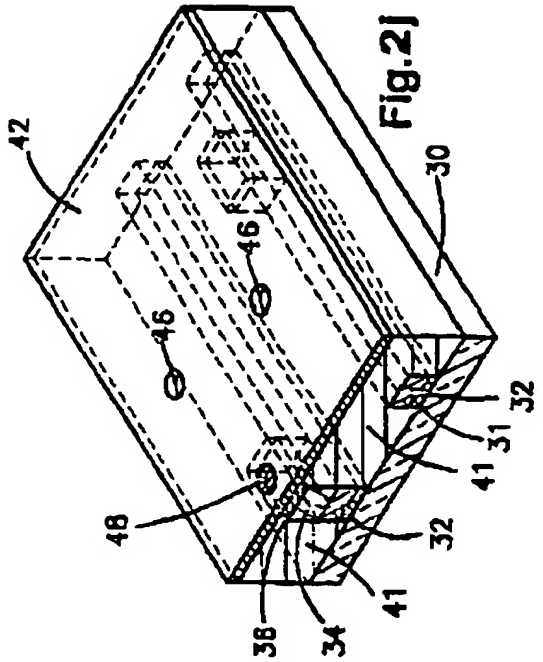

Fig.2j

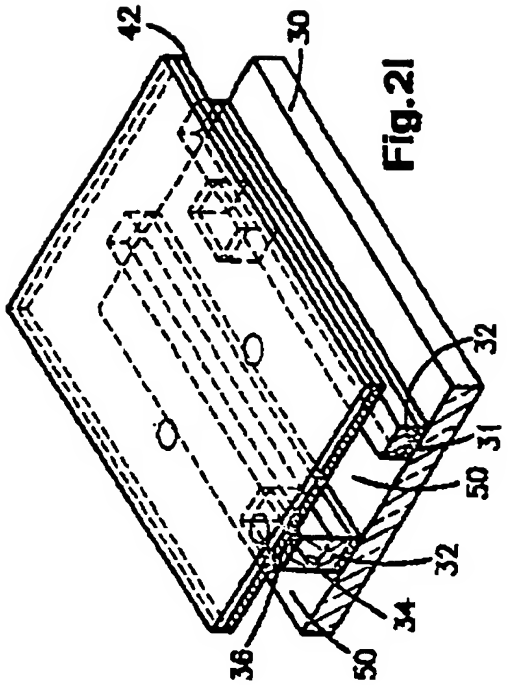

Fig.2l

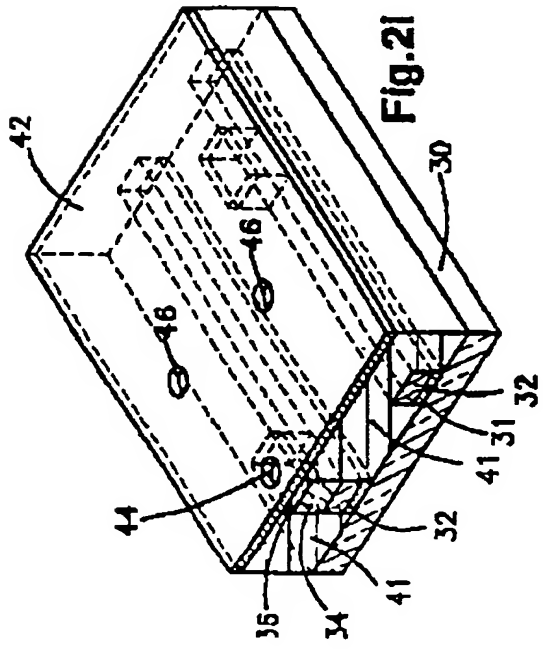

Fig.2l

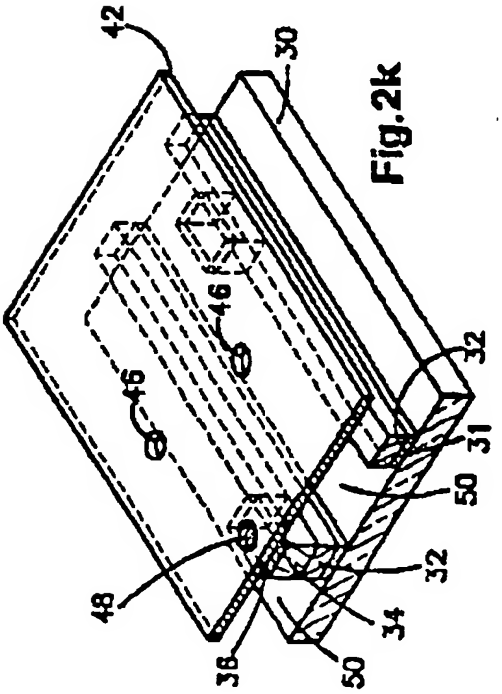

Fig.2k

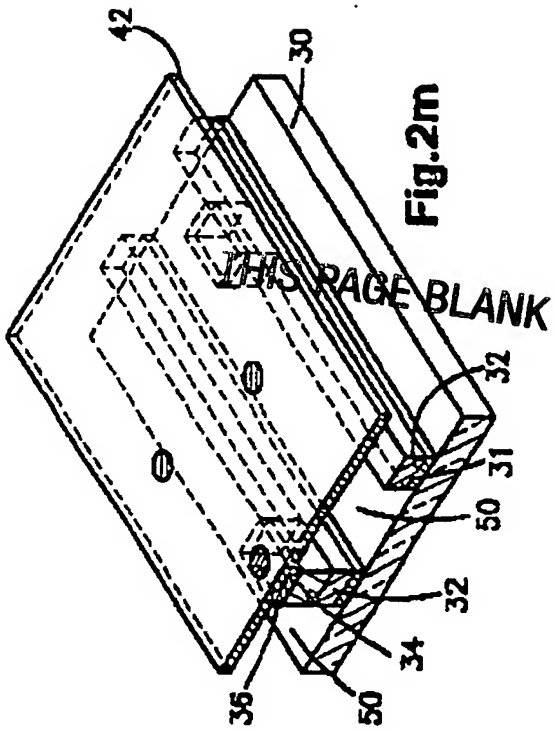

Fig.2m